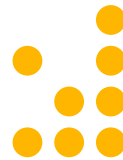


CMPT 478/981 Spring 2025

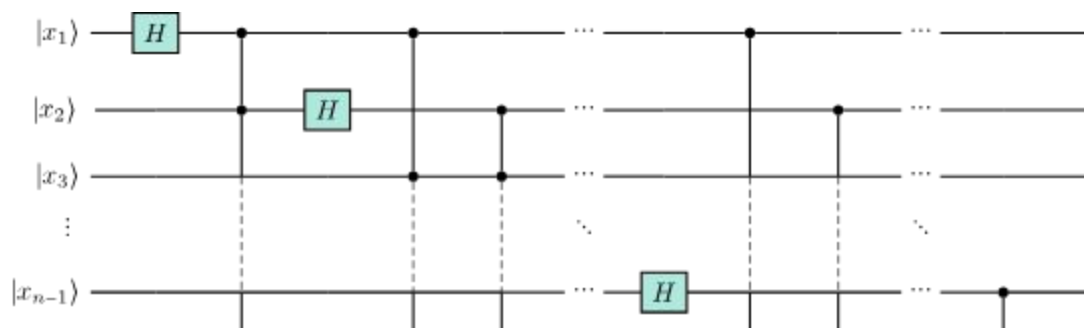
Quantum Circuits & Compilation

Matt Amy

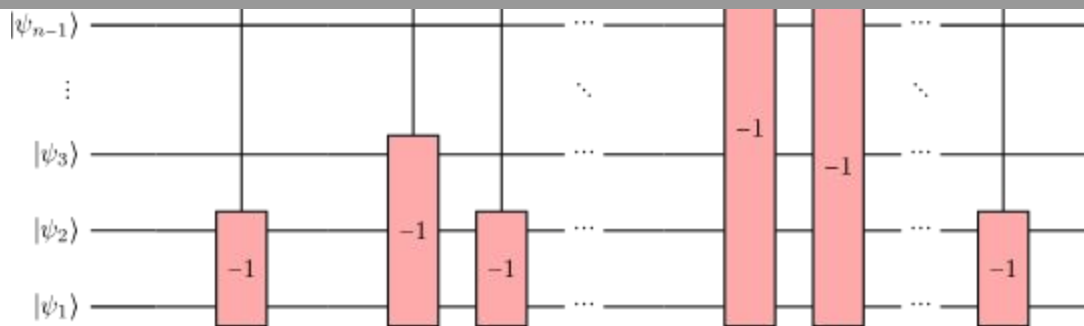
Today's agenda



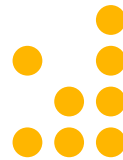
- Paper discussion
- Hardware-specific concerns



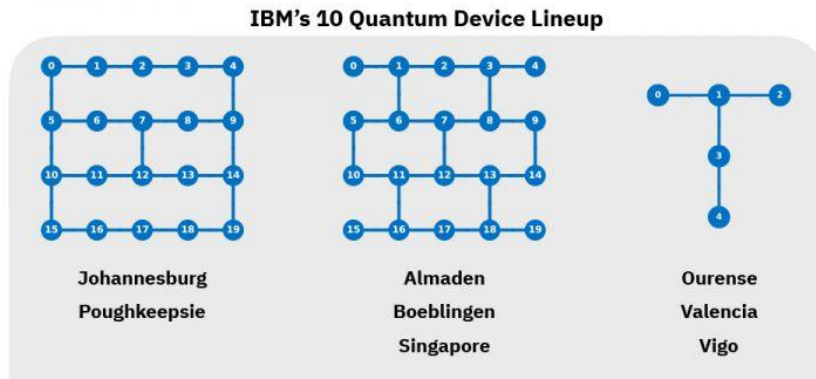
Hardware-aware compilation



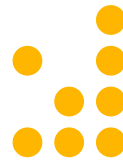
Recall: Topology constraints



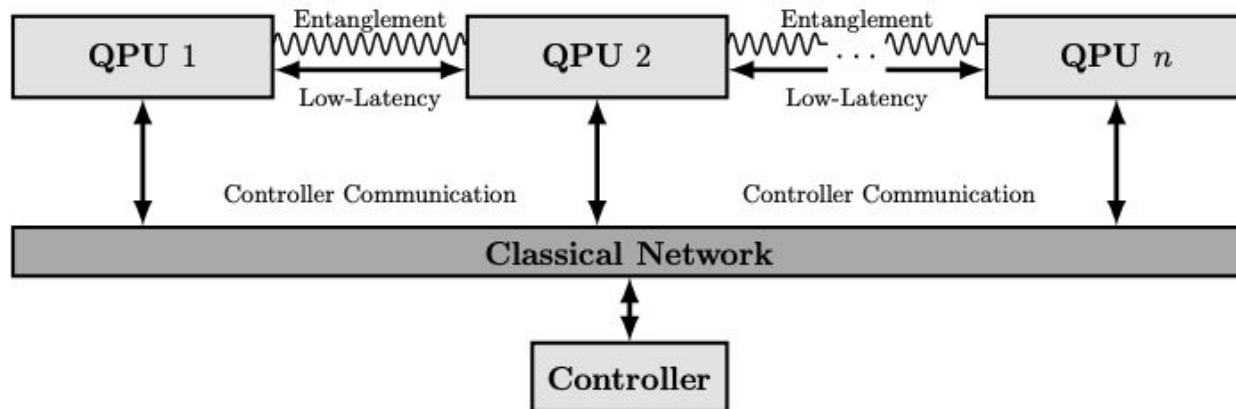
- Next we're going to look at hardware-aware compilation in two contexts:
 - Compiling to near-term devices with gate connectivity constraints, and
 - Compiling to FTQEC devices distributed over many compute nodes with limited **entanglement** connectivity



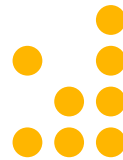
Distributed quantum computing



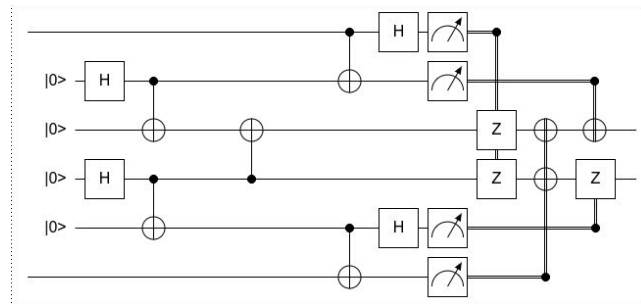
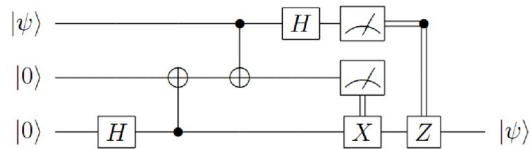
- Addresses scaling QC by having multiple QPUs connected via entanglement
- Connected nodes typically have a source of shared entanglement
 - E.g. halves of a Bell pair prepared as entangled photons and sent to either



Distributing quantum computations



- Assign qubits to QPUs
- When a CNOT gate (or other multi-qubit gate) acts across QPU barriers, have two options:
 - Teleport a qubit from one QPU to the other
 - Teleport the gate **without moving qubits**



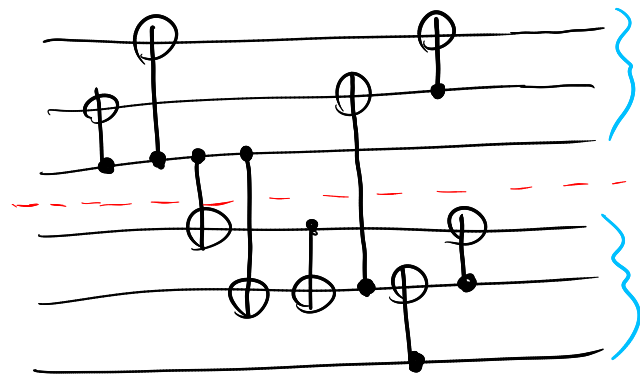
Example

QPU 1

QPU 2



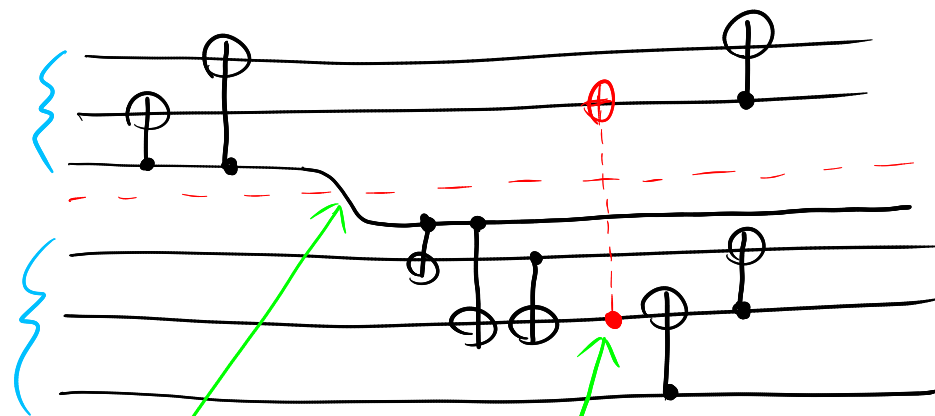
Original circuit



Distributed circuit

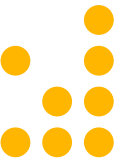
QPU 1

QPU 2



qubit teleportation
(since no more interactions w/ QPU1)

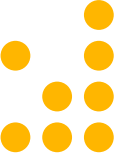
gate teleportation
(since more interactions)



Resource considerations

- QPUs may be distant
- Connected by photons, faced with photon loss
- Need repeaters to ensure reasonable fidelity/rate of photons
- Higher latency compared to in QPU operations
 - → higher error rates as well

Goal (roughly): minimize use of entanglement



Readings for next week

- Posted to the website
 - Li, Ding, Xi, *Tackling the Qubit Mapping Problem for NISQ-Era Quantum Devices*. arXiv:1809.02573
 - Van de griend, Kissinger, *CNOT circuit extraction for topologically-constrained quantum memories*. arXiv:1904.00633
 - Andrés-Martínez, Heunen, *Automated distribution of quantum circuits via hypergraph partitioning*. arXiv:1811.10972
 - Baker, Duckering, Hoover, Chong, *Time-Sliced Quantum Circuit Partitioning for Modular Architectures*. arXiv:2005.12259

- As before send me a short (paragraph or two) summary of **ONE (1)** paper of your choice before next class and be prepared to give a short summary of **any** of the papers in class